WHAT IS CLAIMED IS:

1. A microprocessor built on a semiconductor chip comprising:

a central processing unit for executing instructions; and

an external bus interface control circuit which controls an external bus on the basis of execution of instructions by said central processing unit,

wherein said external bus interface control circuit is capable of selecting one of a plurality of external device select signals corresponding to an external access address and activating said selected external device select signal, and

wherein said microprocessor further comprises a clock switching control circuit for controlling an operation to switch a synchronous clock signal of said external bus interface control circuit in accordance with said external device select signal activated by said external bus interface control circuit.

2. A microprocessor comprising:

a central processing unit for executing instructions; and

an external bus interface control circuit which controls an external bus on the basis of execution of instructions by said central processing unit,

wherein said external bus interface control

circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to an external access address, and

wherein said microprocessor comprises a clock switching control circuit for controlling an operation to switch a synchronous clock signal of said external bus interface control circuit to a first clock signal in accordance with activation of said first external device select signal or to a second clock signal in accordance with activation of said second external device select signal.

3. A microprocessor according to claim 2,

wherein said microprocessor further comprises a clock pulse generator and clock output pins,

wherein said clock pulse generator generates said first clock signal and said second clock signal with a period equal to a predetermined multiple of the period of said first clock signal where said predetermined multiple is defined as a quantity equal to a frequency-division ratio, and

wherein said clock output pins supply respectively said first and second clock signals generated by said clock pulse generator in parallel to respectively outside.

4. A microprocessor comprising:

a central processing unit for executing instructions; and

an external bus interface control circuit controlling an external bus on the basis of execution of instructions by said central processing unit,

wherein said external bus interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to an external access address,

wherein said microprocessor further comprises a clock switching control circuit,

wherein said clock switching control circuit is capable of controlling to switch said synchronous clock signal of said external bus interface control circuit to said first clock signal as well as switch a synchronous clock signal of said central processing unit to a third clock signal in response to activation of said first external device select signal, and is capable of controlling to switch said synchronous clock signal of said external bus interface control circuit to said second clock signal as well as switch said synchronous clock signal of said central processing unit to a fourth clock signal in response to activation of said second external device select signal.

5. A microprocessor according to claim 4, wherein said microprocessor further comprises a

clock pulse generator and clock output pins,

wherein said clock pulse generator generates said first clock signal, said second clock signal with a period equal to a predetermined multiple of the period of said first clock signal where said predetermined multiple is defined as a quantity equal to a frequency-division ratio, said third clock signal and said fourth clock signal with a period equal to another predetermined multiple of the period of said third clock signal where said other predetermined multiple is defined as a quantity equal to another frequency-division ratio,

wherein said clock output pins output respectively said first and second clock signals generated by said clock pulse generator to respectively outside said semiconductor chip, and

wherein said each of frequencies of said third and fourth clock signals is that of said first clock signal.

6. A microprocessor according to claim 2,

wherein said clock switching control circuit requests said central processing unit to suspend execution of instructions in response to activation of a selected external device select signal, and

wherein said clock switching control circuit is further capable of controlling to switch said clock signal after an acknowledgment of a request for suspending of said instruction execution.

7. A microprocessor according to claim 6 wherein said clock switching control circuit is capable of controlling to switch said clock signal at a timing synchronized with periods of said second clock signal.

8. A semiconductor module on a module substrate including a plurality of external connection electrodes and a plurality of wiring layers comprising:

a processor chip; and

a memory chip operating synchronously with a first clock signal,

wherein said microprocessor chip includes a clock pulse generator for generating said first clock signal and a second clock signal with a frequency lower than that of said first clock signal and for supplying in parallel said first and second clock signals to outside,

wherein said microprocessor chip is capable of making an access to said memory chip synchronously with said first clock signal, and

wherein said microprocessor chip is capable of making an external access to outside of said microprocessor chip through one of external connection electrodes synchronously with said second clock signal.

9. A semiconductor module according to claim 8,

wherein said microprocessor chip comprises:

a central processing unit for executing instructions; and

an external bus interface control circuit for controlling an external bus on the basis of execution of an instruction by said central processing unit,

wherein said central processing unit and said external bus interface control circuit are built in a single chip,

wherein said external bus interface control circuit is capable of activating a memory chip select signal for selecting said memory chip in response to an external access address and an external device select signal for selecting a device connected to said microprocessor chip through one of said external connection electrodes,

wherein said microprocessor chip comprises a clock switching control circuit,

wherein said clock switching control circuit is capable of controlling to switch a synchronous clock signal of said external bus interface control circuit to a first clock signal in response to activation of said memory chip select signal, or is capable of controlling to switch said synchronous clock signal of said external bus interface control circuit to a second clock signal in response to activation of said device select signal.

10. A data-processing system comprising:

a first clock wire for transferring a first clock signal;

a second clock wire for transferring a second clock signal with a frequency lower than said first clock signal;

a first device operating synchronously with said first clock signal applying through said first clock wire;

a second device operating synchronously with said second clock signal; and

a third device capable of controlling accesses to said first device synchronously with said first clock signal and capable of controlling accesses to said second device synchronously with said second clock signal,

wherein said first clock wire, said second clock wire, said first device, said second device and said third device are provided on a mounting board.

11. A data-processing system according to claim 10 wherein said mounting board comprises:

a first circuit board including a first board wire connected to said second device; and

a second circuit board including a second board wire connected to said first board wire and said second board wire is connected to said first device and a third device.

12. A data-processing system according to claim 10,

wherein said third device is a microprocessor on a single semiconductor chip comprising a central processing unit for executing instructions, an external bus interface control circuit for controlling an external bus on the basis of execution of instructions by said central processing unit,

wherein said external bus interface control circuit is capable of activating a first external device select signal for selecting said first device or a second external device select signal for selecting said second device in accordance with an external access address,

wherein said third device further includes a clock switching control circuit, and

wherein said clock switching control circuit is capable of controlling to switch a synchronous clock signal of said external bus interface control circuit to a first clock signal in response to activation of said first external device select signal, or is capable of controlling to switch said synchronous clock signal of said external bus interface control circuit to a second clock signal in response to activation of said second external device select signal.

13. A data-processing system according to claim 12,

wherein said third device further comprises a clock pulse generator and clock output pins,

wherein said clock pulse generator applies said first clock signal and said second clock signal with a period equal to a predetermined multiple of the period of said first clock signal where said predetermined multiple is defined as a quantity equal to a frequency-division ratio, and

wherein said clock output pins applies respectively said first and second clock signals generated by said clock pulse generator in parallel to outside said semiconductor chip.

14. A microprocessor according to claim 4,

wherein said clock switching control circuit requests said central processing unit to suspend execution of instructions in response to activation of a selected external device select signal, and

wherein said clock switching control circuit is further capable of controlling to switch said clock signal after an acknowledgment of request for suspending of said instruction execution.